DOWNLOAD PDF HIGH FREQUENCY CIRCUIT DESIGN

Chapter 1 : High Frequency Circuit Design | Download book

In high-frequency circuit design, an important procedure that must be incorporated in every design is matching. The purpose of matching is to prevent signals from being reflected as they move along the various parts of a circuit or system.

December 25, It has good ambient light immunity. Circuit by Dave Johnson P. Circuit by David Johnson P. With the components show, it has a rating of watts max. It too is designed around an inexpensive plastic optical fiber detector. Hobby Circuit designed by David A. Hobby Circuit designed by Dave Johnson P. An opto-coupler provides a very safe 5KV isolation. Circuit by David A. What it lacks in sensitivity it makes up for in speed. The circuit attaches a plastic fiber optic PIN photodiode assembly to a small box containing a small 3v battery and a standard. It has a bandwidth from 1KHz to over 5MHz. It is great for experimenting with various modulated. Output transistors are protected by current-limiting. The design is a good balance between output power, physical size. The completed amplifier will reward the builder with a clean, more powerful output signal for a QRP rig when radio conditions become marginal. This project uses a "classic" RF transistor. With the components show, it has a rating of watts max.. The purpose of this page is to make the circuit diagrams available for educational purposes. Both amplifiers are driven by the input signal and each is configured for a gain of two, one for driving each output cable. The inputs need to have signals centered at 0. The input biasing circuitry is contained on-chip for minimal external component count. A single resistor programs the biasing level of all three channels. There is just one "tricky" component and this is Cx. This component should have an impedance of about ohms at the frequency of interest. If you wish to reduce the transmitter power, increase the value of Cx. It is Cx which causes the square wave from the output transistor to approximate a sine waveform. Ugly-bug construction was used but I dare say that the good results are partly to do with the method of construction. Supply current was a low 2.

Chapter 2 : Design of High Frequency Pulse Transformer

High Frequency Circuit Design by Hardy, James K. and a great selection of similar Used, New and Collectible Books available now at www.nxgvision.com

From time to time, I will hand out problem sets. You must try to work out solutions all on your own. During the tutorials, I will explain some of the problems related to the assignments. Remember assignments do count towards your continual assessments. Please submit solution to Question 2 of Problem Set 1 by 7 October Click this link to see the solution for this assignment. Please submit solution to Question 6 of Problem Set 2 by 28 October The mid-term test will be composed of only ONE problem: Question 3 of Problem Set 3. This forms a "take-home test" to be handed in on 11 November That means each of you will have to reproduce the answer all on your own. Your submission will be counted as mid-semester test. But for Q3 and Q4, they are in triode region. Also, you should know that this total current through Q3 and Q4 plus the current in Q2 must be equal to I1. So, you should be able to get a total of three equations containing the unknowns Veff1, Veff2 and vds3. In part b , you may need to solve this set of equations, requiring numerical solution procedures. Click this link to see the solution for this test. Please submit solution to Question 5 of Problem Set 4 by 25 November See lecture notes for matching procedure. Mini-projects will be done in lieu of laboratory works. There are a few reasons for this. First, many design approaches can be computerised and it is an extremely good exercise for you to develop computer software to aid design. Second, our laboratory is not at the moment well geared towards high-frequency experiments. Third, because our course emphasizes conceptual understanding, mini-projects are good tools to stretch your thinking. The stipulated practical work for this subject is 9 hours of work related to topics taught in the course. I believe it is reasonable to ask you to develop a complete and fully working software to aid the design of high frequency circuits. The 9 hour schedule is the main constraint, which means that I can only specify relatively simple projects. As more topics will be covered as we go along, I suggest that you do a quick preview of the lecture materials to find out if you would like to pursue your mini-project on a topic which will be taught at the later part of the semester. The following topics are arranged in the sequence they are taught. You may choose any ONE of these topics. High frequency roll-off of transistor amplifiers You are required to develop a complete computer software which can generate all poles and zeros, and complete frequency response of the common-emitter amplifier. Your software should input sufficient number of parameters and produce complete list of results. Graphical results would be desirable in the case of frequency responses. A clearly written and complete user manual and a CD-ROM or floppy diskette containing the software will be required in the final submission. Design of matching circuits You are required to develop a complete software which can generate all the circuit component values for the following types of matching circuits: L-circuit, pi-circuit, T-circuit and tapped capacitor circuit. Your software should input sufficient number of parameters e. Transmission line matching You are required to develop a complete software which can generate the information e. Incorporating the Smith chart geometry is preferred over the use of first-principle equations. Note that this is NOT a group project. Each one of you is required to submit a report outlining the objective and your approach together with a CD-ROM or floppy diskette of the software and a complete user manual. The deadline of submission is the day of my last lecture, 2 December I will test your software and verify its functionality, and I will also do a simple "independency check". If two or more of you are found to have submitted essentially the same software, you will get zero mark for this component. There will be a mid-semester test for the purpose of assessment. But it may be more appropriate to do a take-home test which consists of a difficult design problem. This will save a week of lecture time. The written examination will consist of a 2. I will set questions in a way that you will not be able to avoid knowing the basic principles. I will put the basic things in one or two compulsory questions, but will still allow choices so that students with different interests and abilities will be able to pass the examination. Let me stress that I never scale marks! What you get is what you get! So, you should find the paper very answerable if you have followed my course; in other words, I accept no excuse of failure. My time-table is posted outside my office. But since our class is on every Friday, it seems to be convenient if you can see me if you have a question about your study in the afternoon before the lecture starts. This will allow me to replicate interesting problems to the whole class, if it is appropriate to do so. Also, Friday afternoons will be more convenient for part-timers as they may just drop in a bit earlier in the same evening. Friday 3pm to 6 pm.

Chapter 3 : IEEEtv | Technology | High Frequency Magnetic Circuit Design for Power Electronics

High Frequency Circuit Design by Prof. Michael Tse File Type: Online Number of Pages: NA Description This lecture note will look mainly at circuit design in the tens-hundreds MHz range and will touch upon some basics for the GHz range design.

Furthermore, the Dresden location features the "Silicon Saxony", which is the largest microelectronics cluster in Europe. April and is fix termed until The position offers the chance to obtain further academic qualification e. The Chair of Circuit Design and Network Theory is a leading Chair in the design of radio frequency and millimeter-wave integrated circuits and has received several world records and awards e. The project is e. Your task will be the development analysis, simulation, layout, measurement and optimiza-tion of the adaptive integrated chip frontend in BiCMOS technology. Among the key components of the transmitter to be developed are the power amplifier, the up-mixer, the vector modulator for beamforming control and the oscillator interface. Furthermore you contribute to system integration and tests, will publish scientific papers and attend project meetings and conferences. The job offer provides an excellent platform for interdisciplinary cooperation and the ability to push your personal scientific development. Applications from women are particularly welcome. The same applies to people with disabilities. Please send your complete application including copies of your CV and certificates until Please submit copies only, as your application will not be returned to you. Expenses incurred in attending interviews cannot be reimbursed. Reference to data protection: Your data protection rights, the purpose for which your data will be pro-cessed, as well as further information about data protection is available to you on the website: We are looking for a candidate with a very good or good university degree in electrical engineering, communications technology or information technology with profound knowledge in analog circuit design. For that, skills are especially needed in CAD-based circuit simulations and circuit layout. Knowledge in radio frequency and if possible millimeter-wave circuit design would be advantageous. Interest in new technologies, independent and flexible way of working, communication and teamwork skills, good English, innovative and analytical thinking and high commitment are expected.

Chapter 4 : Amplifier Circuits: High Frequency / High Speed

The Future ofHigh Frequency Circuit Design InvitedPaper Ali Hajimiri California Institute ofTechnology, such high-frequency complex circuits implemented in silicon.

The main purpose of transformer is to either step up or step down the voltage level of power at various point of network for efficient power transmission and distribution. The power at generating stations is generated at low voltage and high current so as to minimize the ohmic loss in the lines and to transfer the power to the load centers with less power loss efficiently this low voltage level of power is to be stepped up to reduce line current hence to reduce ohmic loses and to get better voltage regulation. Since in this journey of power from generating stations to the load centers, due to line resistance there will be ohmic loss and due to the line impedance there will be voltage fall or poor voltage regulation. For efficient distribution and supply this high voltage power is again stepped down at desired distribution and supply voltage level. All the way the frequency of the transformer and power remain constant. What is High frequency Transformers or Pulse Transformer As the name prefaces the operating frequency of these transformers would be typically around few hundred kilo hertz. One such energy efficient device is High Frequency Pulse Transformer. The switching frequency of these SMPSs Switched Mode Power Supply system will be very high as a concern it reduces the size of magnetics like transformer and inductor and and it reduces the ripple and so on. In later sessions we will be discussing about complete design of High frequency transformer from fundamentals for a DC-DC converter as an application. To match the voltage levels of Source and the Load To provide electrical isolation between the power circuits. Also as the flux divides in the outer limbs it offers less core losses. The commonly used shell core is EE - Core. Commonly for frequencies less than 5 MHz manganese-zinc ferrites are used above which nickel-zinc ferrites are of common choice. Only concern with ferrites is its operating maximum flux density is limited to maximum of 0. The high frequency transformers are also called Pulse transformer as the input voltage wave form commonly applied to it is a pulse train as depicted in the figure below. The flux waveform is also shown in it which is integral of voltage waveform from the relation Faradays law of electromagnetic induction. B Secondly we shall derive an equation for Aw Window Area: As discussed earlier Window area of a transformer provides accommodation for primary and secondary winding. But entire window area is not used for the winding a portion of it is used for insulation therefore a factor Kw is introduced which is called window space factor or window utilization factor. High Frequency 50 kHz Application. Now we need to design transformer for above application, Assumptions: From the equation 3 that we have derived, there substituting all the values and finding the value of window and core area. After we derive this value, from the data sheets of the Core we need to select the appropriate core.

Chapter 5 : A Practical Guide to High-Speed Printed-Circuit-Board Layout | Analog Devices

An integral part of any communications system, high-frequency and microwave design stimulates major progress in the wireless world and continues to serve as a foundation for the commercial wireless products we use every day. The exceptional pace of advancement in developing these systems stipulates.

There are many aspects to high-speed PCB layout; volumes have been written on the subject. This article addresses high-speed layout from a practical perspective. A major aim is to help sensitize newcomers to the many and various considerations they need to address when designing board layouts for high-speed circuitry. But it is also intended as a refresher to benefit those who have been away from board layout for a while. Not every topic can be covered in detail in the space available here, but we address key areas that can have the greatest payoff in improving circuit performance, reducing design time, and minimizing time-consuming revisions. Although the focus is on circuits involving high-speed op amps, the topics and techniques discussed here are generally applicable to layout of most other high-speed analog circuits. When op amps operate at high RF frequencies, circuit performance is heavily dependent on the board layout. Thinking ahead and paying attention to salient details throughout the layout process will help ensure that the circuit performs as expected. The Schematic Although there is no guarantee, a good layout starts with a good schematic. Be thoughtful and generous when drawing a schematic, and think about signal flow through the circuit. A schematic that has a natural and steady flow from left to right will tend to have a good flow on the board as well. Put as much useful information on the schematic as possible. The designers, technicians, and engineers who will work on this job will be most appreciative, including us; at times we are asked by customers to help with a circuit because the designer is no longer there. What kind of information belongs on a schematic besides the usual reference designators, power dissipations, and tolerances? Here are a few suggestions that can turn an ordinary schematic into a superschematic! Add waveforms, mechanical information about the housing or enclosure, trace lengths, keep-out areas; designate which components need to be on top of the board; include tuning information, component value ranges, thermal information, controlled impedance lines, notes, brief circuit operating descriptions â€¦ and the list goes on. An ounce of prevention at this point is worth more than a pound of cure! Your inputs and guidance are most critical at the beginning of the layout process. The more information you can provide, and the more involved you are throughout the layout process, the better the board will turn out. Give the designer interim completion pointsâ€”at which you want to be notified of the layout progress for a quick review. Your instructions for the designer should include: About 10 years ago I designed a multilayer surface-mounted boardâ€”with components on both sides of the board. The board was screwed into a gold-plated aluminum housing with many screws because of a stringent vibration spec. Bias feed-through pins poked up through the board. The pins were wire-bonded to the PCB. It was a complicated assembly. Some of the components on the board were to be SAT set at test. Can you guess where some of them were placed? On the bottom of the board. The production engineers and technicians were not very happy when they had to tear the assembly apart, set the values, and then reassemble everything. Location, Location, Location As in real estate, location is everything. Where a circuit is placed on a board, where the individual circuit components are located, and what other circuits are in the neighborhood are all critical. Start with critical component placement, in terms of both individual circuits and the entire board. Getting it right the first time lowers cost and stressâ€”and reduces cycle time. There are two commonly used configurations for bypassing high-speed op amps. Typically, two parallel capacitors are sufficientâ€—but some circuits may benefit from additional capacitors in parallel. Paralleling different capacitor values helps ensure that the power supply pins see a low ac impedance across a wide band of frequencies. This is especially important at frequencies where the op-amp power-supply rejection PSR is rolling off. Figure 1 shows the benefits of multiple parallel capacitors. At lower frequencies the larger capacitors offer a low impedance path to ground. Once those capacitors reach self resonance, the capacitive quality diminishes and the capacitors become inductive. That is why it is important to use multiple capacitors: The ground side of the capacitor should be connected into the ground plane with minimal lead- or trace length. Figure 2 illustrates this technique. This process should be repeated for the next-higher-value capacitor. A good place to start is with 0. An alternate configuration uses one or more bypass capacitors tied between the positive- and negative supply rails of the op amp. This method is typically used when it is difficult to get all four capacitors in the circuit. A drawback to this approach is that the capacitor case size can become larger, because the voltage across the capacitor is double that of the single-supply bypassing method. The higher voltage requires a higher breakdown rating, which translates into a larger case size. This option can, however, offer improvements to both PSR and distortion performance. Since each circuit and layout is different; the configuration, number, and values of the capacitors are determined by the actual circuit requirements. Parasitics Parasitics are those nasty little gremlins that creep into your PCB quite literally and wreak havoc within your circuit. They are the hidden stray capacitors and inductors that infiltrate high-speed circuits. They include inductors formed by package leads and excess trace lengths; pad-to-ground, pad-to-power-plane, and pad-to-trace capacitors; interactions with vias, and many more possibilities. Figure 3 a is a typical schematic of a noninverting op amp. If parasitic elements were to be taken into account, however, the same circuit would look like Figure 3 b. Typical op amp circuit, as designed a and with parasitics b. Sometimes just a few tenths of a picofarad is enough. If enough capacitance is present, it can cause instability and oscillations. Additional peaking caused by parasitic capacitance. A few basic formulas for calculating the size of those gremlins can come in handy when seeking the sources of the problematic parasitics. Equation 1 is the formula for a parallel-plate capacitor see Figure 5. Capacitance between two plates. Strip inductance is another parasitic to be considered, resulting from excessive trace length and lack of ground plane. Equation 2 shows the formula for trace inductance. All dimensions are in millimeters. Inductance of a trace length. The oscillation in Figure 7 shows the effect of a 2. The equivalent stray inductance is 29 nH nanohenry , enough to cause a sustained low-level oscillation that persists throughout the period of the transient response. The picture also shows how using a ground plane mitigates the effects of stray inductance. Pulse response with â€”and withoutâ€”ground plane. Vias are another source of parasitics; they can introduce both inductance and capacitance. Equation 3 is the formula for parasitic inductance see Figure 8. Equation 4 shows how to calculate the parasitic capacitance of a via see Figure 8. T is the thickness of the board. D1 is the diameter of the pad surrounding the via. D2 is the diameter of the clearance hole in the ground plane. All dimensions are in centimeters. A single via in a 0. A list of references appears at the end of this article. A ground plane acts as a common reference voltage, provides shielding, enables heat dissipation, and reduces stray inductance but it also increases parasitic capacitance. While there are many advantages to using a ground plane, care must be taken when implementing it, because there are limitations to what it can and cannot do. Ideally, one layer of the PCB should be dedicated to serve as the ground plane. Best results will occur when the entire plane is unbroken. Resist the temptation to remove areas of the ground plane for routing other signals on this dedicated layer. The ground plane reduces trace inductance by magnetic-field cancellation between the conductor and the ground plane. When areas of the ground plane are removed, unexpected parasitic inductance can be introduced into the traces above or below the ground plane. Because ground planes typically have large surface and cross-sectional areas, the resistance in the ground plane is kept to a minimum. At low frequencies, current will take the path of least resistance, but at high frequencies current follows the path of least impedance. Nevertheless, there are exceptions, and sometimes less ground plane is better. High-speed op amps will perform better if the ground plane is removed from under the input and output pads. Capacitive loading at the outputâ€”including straysâ€”creates a pole in the feedback loop. This can reduce phase margin and could cause the circuit to become unstable. Analog and digital circuitry, including grounds and ground planes, should be kept separate when possible. Fast-rising edges create current spikes flowing in the ground plane. These fast current spikes create noise that can corrupt analog performance. Analog and digital grounds and supplies should be tied at one common ground point to minimize circulating digital and analog ground currents and noise. At high frequencies, a phenomenon called skin effect must be considered.

Chapter 6 : EIE High Frequency Circuit Design Homepage www.nxgvision.com

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Documents for RF Circuit Designs (Focusing on using Advance Design System (ADS) Software) and High-Speed PCB Design The information provided here has been obtained from sources believed to be reliable.

Chapter 7 : High Frequency/RF Circuit Design

graduate-level course in radio frequency circuit design at the University of Texas at Arlington. This class has continued to be popular for the past 20 years under.

Chapter 8 : Research Associate / Phd Student In High Frequency Circuit Design

in High Frequency Circuit Design (Subject to personal qualification employees are remunerated according to salary group E 13 TV-L) The position starts at 1st April and is fix termed until 31st March

Chapter 9 : High Frequency Circuit Design by James K. Hardy

Insulated Wire Inc. is pleased to announce that following the retirement of a French delegate, IW Microwave Products Division President, John Morelli, has been appointed as the Secretary for IEC/SC46F, a subcommittee of IEC/TC